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ESE (Mains) 2019
Electronic Measurement & Instrumentation

Important Questions with Solutions

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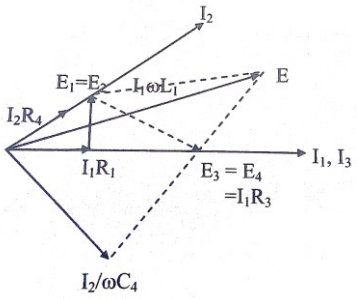
1. Draw a neat circuit diagram along with phasor diagram of a Wien-bridge circuit for measuring unknown frequencies in the audio range. What are the advantages of this bridge circuit over other methods for measurement of frequency?

Wien Bridge:



Phasor diagram

Under balanced conditions

$$\left(\frac{R_1}{1+j\omega C_1R_1}\right)R_4=\left(R_2-\frac{j}{\omega C_2}\right)R_3$$

$$\frac{R_4}{R_3}=\frac{R_2}{R_1}+\frac{C_1}{C_2}+j\left(\omega C_1R_2-\frac{1}{\omega C_2R_1}\right)$$

$$\frac{R_4}{R_3}=\frac{R_2}{R_1}+\frac{C_1}{C_2}$$

And $\omega=C_1R_2=\frac{1}{\omega C_2R_1}$

$$\omega=\frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$f=\frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}Hz$$

If $R_1 = R_2$ and $C_1 = C_1 = C_2 = C$

$$f=\frac{1}{2\pi RC},\frac{R_4}{R_3}=2$$

Advantages:

i) The Wien bridge oscillator provides a stable, low distortion sinusoidal outputvoltage over a wide range of frequency

ii) The frequency range can be selected by using simple decade resistance boxes.

iii) The frequency of oscillation in an RC network is $f_0=\frac{1}{2\pi RC}$ This, unlike L-C networks where the resonant frequency varies inversely as square root of C,the frequency of Wien bridge oscillator varies inversely as C itself. Thusfrequency variation greater than 10:1 is possible with single sweep of an airdielectric tuning capacitor.

iv) With the addition of the power amplifier to isolate the oscillator from the load,the circuit is used to provide test signals for a variety of applications.

v) The range of this oscillator is 2 Hz to 100 kHz. The upper frequency limit isfixed by the amplitude and the phase shift characteristics of the amplifier. Thelower limit of frequency is fixed by the practical limits on the size of range selecting resistors.

2. The e.m.f. of standard cell used for standardization is 1.0183 volts. If the balances is obtained at a length of 55 cm, determine:

(i) The e.m.f. of the cell which balances at 80 cm.

(ii) The current flowing through a standard resistance of 2Ω if the p. d across it balance at 65 cm

(iii)The voltage of a supply main which is reduced by a volt-ratio box to one hundredth and balance is obtained at 85 cm
(iv) The percentage error in ammeter reading 0.35 ampere when balance is obtained at 45 cm with the p. d. across a 2.5Ω resistor in the ammeter; circuit
(v) The percentage error in a voltmeter reading 1.42 volts when balance is obtained at 75 cm

Solution:

Given: e.m.f. of the standard cell 1.0183 V
The voltage drop per cm length of potentiometer wire,

$$v = \frac{1.0183}{55} = 0.0185145$$

(i) The e.m.f. of a cell which balances at 70 cm
= v. I = 0.0185145 × 70 = 1.48116 volts
(ii) The potential difference which balances at 65 cm
= v. l = 0.0185145 × 65 = 1.20344 volts
Magnitude of the standard resistor. S = 2Ω

Current flowing through 2Ω resistance $= \frac{V}{S} = \frac{1.20344}{2} volts = 0.60172$

(iii) The p.d which balances at 85 cm,
= V = v. I = 0.0185145 × 85 = 1.57373 volts
Voltage of supply main = V × Ratio of volt- ratio box
= 1.57373 × 100 = 157.373 volts
(iv) The p.d which balances at 45 cm,
V = v. I = 0.0185145 × 45 = 0.83315 volts
Current through 2.5 Ω resistance,

$$I = \frac{V}{S} = \frac{0.83315}{2.5} = 0.33326A$$

Percentage error in ammeter reading

$$= \frac{0.35 - 0.33326}{0.33326} \times 100 = 5\% high$$

(v) The p.d. which balances at 75 cm
= 0.0185145 × 75 = 1.38859 Volts
Voltmeter reading = 1.42 volts
Percentage error in voltmeter reading

$$= \frac{1.42 - 1.38859}{1.38859} \times 100 = 2.26\% high$$

3. A barium titanate piezoelectric pickup has dimensions of 5 mm × 5 mm × 1.5 mm and a voltage sensitivity of 0.014 Vm/N. Determine the voltage developed when a force of 0.7 kg is applied to it. Determine also the charge sensitivity if the relative permittivity of the barium titanate is 1600.

Solution:

Voltage sensitivity, g = 0.014 V m/N
Thickness, t = 1.5 mm = 1.5 × 10^{-3} m
Force applied, F = 0.7 kg = 0.7 × 9.81 N
Area of plates, A = 5 × 5 mm^2 = 25 × 10^{-6} m^2

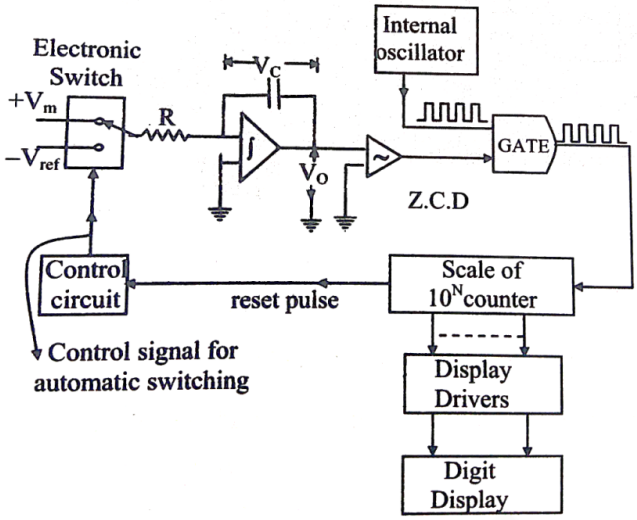
Voltage developed, $V_{out} = gt \times \frac{F}{A}$

$$= \frac{0.014 \times 1.5 \times 10^{-3} \times 0.7 \times 9.81}{25 \times 10^{-6}} = 5.76828V$$

Relative permittivity $\varepsilon_r = 1600$

Charge sensitivity, d = $\varepsilon_0 \varepsilon_r$ g
= 8.854 × 10^{-12} × 1600 × 0.014 = 198.3296 pC/N

4. With a neat sketch, explain dual slope integrating type digital voltmeter
Solution:
Principle of operation:
Dual slope integrating type DVM works on the principle of "Voltage to time conversion". An integrating capacitor is charged for a fixed time period and then discharged with a fixed current.
Functional block diagram:



V_m = Analog DC voltage to be measured
V_{ref} = Reference voltage
F = Frequency of clock pulses generated by internal clock generator
N = No. of Digits in the display
V_C = voltage across integrating capacitor
V_o = output voltage of integrator
R & C are Integrator's Resistance & Capacitance Values
Operation:
At t =0, integrator is connected to "V_m" by throwing the electronic switch manually in up direction

As such, the integrating capacitor starts charging with a variable current $\left(\frac{V_m}{R}\right)$. ZCD produced a start pulse at t = 0, since V_0crosses 0V. This start pulse opens the GATE and in turn clock pulses generated internally pass through the GATE. Counting these clock pulses from t = 0 onwards.
This counter is allowed to count up to "full count" irrespective of $|V_m|$. say, At t = t_1, counter has reached to its full count and overflows. The reset pulse produced by counter is feedback to input side and used to throw the electronic switch in down direction automatically
At t = $t_1$integrator is connected to "-Vref" automatically due to counter overflow.

Now, the integrating capacitor starts discharging with a fixed current $\left(\frac{V_{ref}}{R}\right)$.

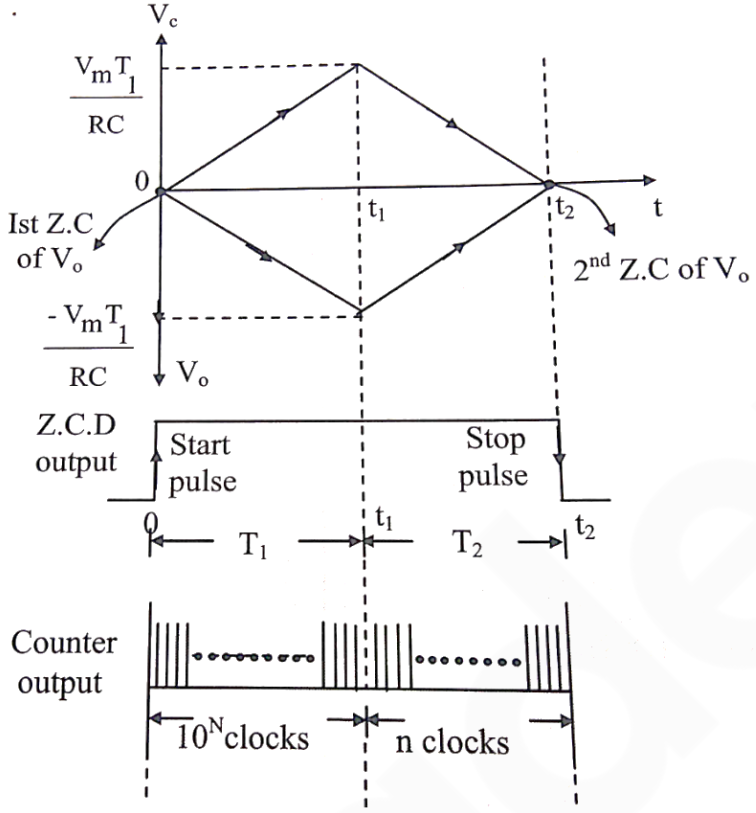
The clock pulses are still allowed to pass through the GATE as it is open (i.e., not affected by counter overflow). Counter restarts counting and continues to count — up. Once the capacitor is completely discharged at t_2, Z.C. D produces a stop pulse since V_o. crosses OV for the 2nd time. This stop pulse closes the GATE and in turn clock pulses are not allowed to pass through the GATE.
Counter stops counting at t = t_2.
Say, the accumulated count is 'n'
Relation & between V_m & n

Period	output of integrator
$At\ t=0$	$V_o=0\left(1^{st}\ zero\ crossing\ \right)$
$0<t<t_1$ $\leftarrow T_1\rightarrow$	$V_o=\frac{1}{RC}\int_{-\infty}^{t_1}V_m$ $=\frac{-V_m}{RC}\int_0^{t_1}dt$ $(\because \quad \text{ıg}\ \ zero\ initial\ voltage)$
$At\ t=t_1$	$V_{01}=-\frac{V_m}{RC}\times(t_1-0)$ $\Rightarrow V_{01}=-\frac{V_m}{RC}T_1.....(1)$
$t_1<t<t_2$	$V_0=\frac{-1}{RC}\int_{-\infty}^{t_2}\left(-V_{ref}\right)dt=0+V01+$ $\frac{1}{RC}\int_{t_1}^{t_2}V_{ref}dt$ $V_o=\frac{V_{ref}}{RC}\int_{t_1}^{t_2}dt+V_{01}$
$At\ t=t_2$	$V_{02}=0$ $\Rightarrow\frac{V_{ref}}{RC}\times(t_2-t_1)+V_{01}=0$ $\Rightarrow\frac{V_{ref}}{RC}\times T_2-\frac{V_m}{RC}T_1=0$ $\Rightarrow\frac{V_m}{RC}T_1=\frac{V_{ref}}{RC}T_2$ $\Rightarrow V_mT_1=V_{ref}T_2$
	$\Rightarrow V_m=\left[\frac{V_{ref}}{T_1}\right]\times T_2$ *Where,* $T_1=1^{st}$ integration time period $=$ Deintegration time period $=n\times t_{clk}$ $V_m=\frac{V_{ref}}{10^N\times t_{clk}}\times n\times t_{clk}$ $\Rightarrow V_m=\left[\frac{V_{ref}}{10^N}\right]\times N$

Features of Dual slope Integrating DVM:

- High measurement accuracy
- High noise rejection
- High stability
- Less hardware complexity
- High conversion time & low operating speed.

Timing waveforms:



Advantages of dual slope DVM

In this DVM, $V_m = \frac{V_{ref}}{10^N} \times n$

There is no dependency on R, C, t_{clk}.

The only possible source of error is reference voltage, This DVM can be designed to offer high measurement accuracy if a highly stable DC source is provided in the design.

- Dual slope integrating DVM measures true average value of input. As such, and AC component riding on DC voltage to be measured (supply noise or power line noise) will be averaged out to zero. This is due to integration carried out on V_m for fixed time period.
- Dual slope integration DVM offers high nose- rejection and is highly stable even if used in noise environment
- Dual slope integration DVM has less hardware complexity compared to other DVMS.

Design criterion to reject power line noise

$T_1 \geq T_s$ i.e. $T_1 = n\ T_s$

Where.

T_1 = 1st integration time period

T_2 = Time period of sinusoidal component riding on DC voltage to be measured n ≥ 1

Ex: The integrating time interval recommended for integrating A/D converter to

$$T_{1(\min)} = 1 \times T_s = 1 \times \frac{1}{50Hz} = 20ms$$

Disadvantage:
The disadvantage of dual slope type DVM is its Operating speed.
Conversion time = $T_1 + T_2 = (10^N + n)t_{clk}$
Dual slope DVM has high conversion time. As much, it is the slowest DVM compared to other types.

5. A coil was tested using a Q- meter and the following results were obtained.

Oscillator frequency	*Tuning capacitance setting*
$2MHz$	$200PF$
$4MHz$	$40PF$

Find the self capacitance of the coil.

Solution:
Given that: f_1 = 2MHz & C_1 = 200PF
f_2 = 4MHz & C_2 = 40PF

$$\therefore n = \frac{f_2}{f_2} = 4MHz / 2MHz = 2$$

After inserting the test coil into socked of Q – meter, the resonance is obtained for the first time at 2MHz with tuning capacitance set to 200pF. Then, the frequency is doubled (i.e., n = 2) and, the resonance is obtained for the second time at 6MHZ with tuning capacitance set to 40pF.

We know: $C_d = \frac{C_1 - n^2 C_2}{n^2 - 1}$

$$= \frac{200pF - (2)^2 40pF}{(2)^2 - 1}$$

$$= \frac{200pF - 160pF}{3}$$

C_d = 13.33pF.
The self capacitance or distributed capacitance of coil is found to be 13.33pF.